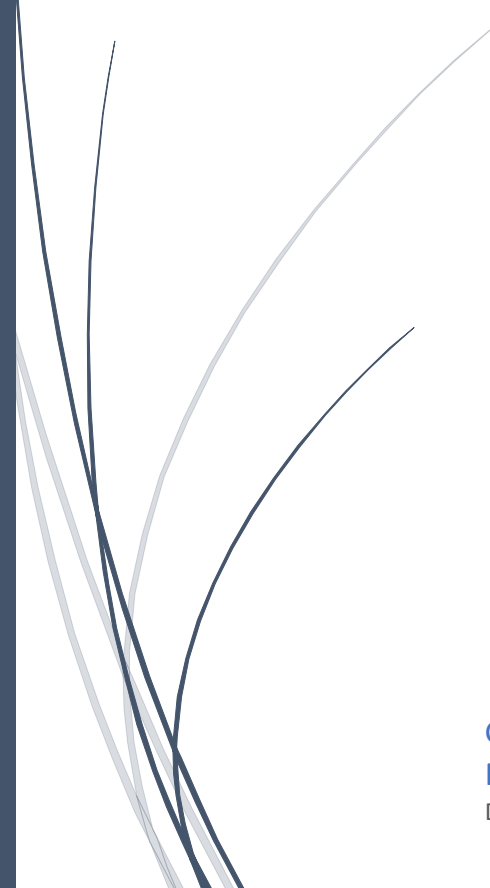


The logo for RADemics, featuring the text "RADemics" in white on a blue arrow-shaped background pointing to the right. The arrow is part of a larger blue horizontal bar that is attached to a dark blue vertical bar on the left side of the page.

RADemics

# IoT Enabled Smart Sensing Systems Using RISC V Based Microcontrollers and Embedded AI

A decorative graphic consisting of several thin, curved lines in shades of blue and grey, originating from the bottom left and extending upwards and to the right, resembling stylized grass or reeds.

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# IoT Enabled Smart Sensing Systems Using RISC V Based Microcontrollers and Embedded AI

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## Abstract

This chapter presents an in-depth exploration of IoT-enabled smart sensing systems leveraging RISC-V based microcontrollers integrated with embedded artificial intelligence (AI). The flexible and open-source nature of the RISC-V architecture facilitates the development of customizable, low-power processors tailored to meet the stringent requirements of edge intelligence in diverse IoT applications. Key challenges addressed include optimizing hardware-software co-design, adapting lightweight AI models such as CNNs and RNNs for constrained memory footprints, and implementing microarchitectural enhancements to achieve low-latency inference. The chapter investigates real-time scheduling and task partitioning strategies essential for concurrent AI execution on resource-limited devices. Emphasis is placed on benchmarking methodologies using open datasets and standardized testing protocols to ensure reliable performance evaluation. This comprehensive overview provides valuable insights into design methodologies, deployment workflows, and performance optimization techniques critical for advancing intelligent sensing solutions in power-sensitive and latency-critical IoT environments.

**Keywords:** RISC-V microcontrollers, embedded AI, IoT smart sensing, hardware-software co-design, low-latency inference, real-time scheduling

## Introduction

The rapid expansion of the Internet of Things (IoT) ecosystem has transformed the manner in which data is collected, processed, and utilized across various domains, including industrial automation, environmental monitoring, healthcare, and smart cities [1]. Central to these developments are smart sensing systems that act as the primary interface between physical phenomena and digital intelligence [2]. These systems require efficient processing capabilities capable of handling heterogeneous sensor data, often under stringent constraints such as limited power supply, compact form factors, and real-time responsiveness [3]. Traditional microcontroller architectures struggle to meet these demands due to their fixed instruction sets and limited scalability. This has intensified interest in open and customizable processor designs that can be tailored to specific application requirements, with RISC-V emerging as a compelling alternative

[4]. The open-source nature of RISC-V enables extensive flexibility in instruction set customization, facilitating the integration of embedded artificial intelligence (AI) capabilities directly within edge devices, thereby reducing reliance on cloud-based processing and minimizing latency [5].

RISC-V based microcontrollers have gained significant traction in recent years due to their modular design philosophy, which allows for the selective inclusion of instruction set extensions aligned with the functional needs of smart sensing applications [6]. This adaptability not only promotes energy-efficient designs by eliminating unnecessary circuitry but also supports the integration of AI accelerators and specialized computation units [7]. Embedded AI algorithms deployed on these microcontrollers enable autonomous decision-making, anomaly detection, and predictive analytics in real time, all within the confines of limited computational resources [8]. By localizing inference processes, these systems significantly reduce data transmission overhead, conserve bandwidth, and enhance privacy [9]. Nonetheless, challenges remain in optimizing hardware-software co-design to balance computational efficiency, memory utilization, and energy consumption, especially given the limited memory and processing capabilities inherent in microcontroller-class devices [10].